**University of engineering & technology Peshawar**



**Circuit & system-1**

**Lab report # 5**

**Fall 2020**

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**Section: B**

**Reg No: 19PWCSE1795**

**Semester: 2nd**

**Submitted to:**

**Eng: faizullah**

**Department Of Computer System Engineering**

**Rubrics of lab**

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| **LAB REPORT ASSESSMENT** | | | | | | | |
| **Criteria** | **Excellent** | **Average** | | **Nill** | | **Marks Obtained** | |
| 1. **Objectives of Lab** | All objectives of lab are properly covered  [Marks 0.5] | Objectives of lab are partially covered  [Marks 0.25] | | Objectives of lab are not shown  [Marks 0] | |  | |
| 1. **Kirchoff’s Voltage Law, Kirchoff’s Current Law, Ohm’s Law.**   **(Statement, Mathematical Expression, Circuit Diagram)** | Correct KVL, KCL and Ohm’s Law statement and mathematical expression is written. Circuit diagram shown is correct and properly labeled  [Marks 1] | | KCL statement or mathematical expression or circuit diagram is missing or circuit diagram is not properly labeled  [Marks 0.5] | | |  | |
| 1. **Apparatus Used** | All equipment and electrical components used are shown  [Marks 1] | Equipment and electrical components are partially shown and some of the components are missing [Marks 0.5] | | Equipment and electrical components used are not shown  [Marks 0] |  | |  |
| 1. **Procedure** | All experimental steps are shown in detail  [Marks 1.5] | Some of the experimental steps are missing      [Marks 1] | | Experimental steps are missing  [Marks 0] |  | |  |
| 1. **Observations & Calculations** 2. **Verification of KCL** 3. **Verification of KVL** 4. **Verification of Ohm’s Law** | All experimental results are completely shown in form of table for all given laws. Error calculation between theoretical and practical values are also shown  [Marks 3] | Experimental results are partially shown and some of the observations are missing and no error calculation is shown  [Marks 1.5] | | No experimental results are shown  [Marks 0] | |  | |
| 1. **Analysis** 2. **Analysis about KVL** 3. **Analysis about KCL** 4. **Analysis about Ohm’s Law** | Analysis and discussion about all experimental results are shown  [Marks 3] | Analysis and discussion about experimental results are partially shown  [Marks 1.5] | | Analysis is not shown  [Marks 0] | |  | |
| Total Marks Obtained:\_\_\_\_\_\_\_\_\_\_                                                                 Instructor Signature: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ | | | | | | | |
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**Complex Circuit Analysis using Breadboard**

1. **Objectives:**

* To verify all basic laws of circuits and systems on complex circuit on breadboard and to do comprehensive analysis from observations.
* Also analyze differences in theoretical and practical readings.
* To know about breadboard .
* To know about complex circuit.

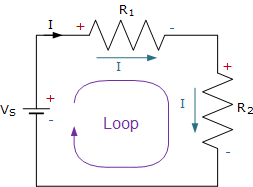
1. **A) Kirchhoff’s Voltage Law:**

* Kerchief voltage law is also known as law of conservation of energy.
* KVL depends upon the concept of a loop.
* A loop is any closed path through the circuit which encounters no node more than once. Essentially, to create a loop, start at any node in the circuit and trace a path through the circuit until you get back to your original node.

**Statement:**

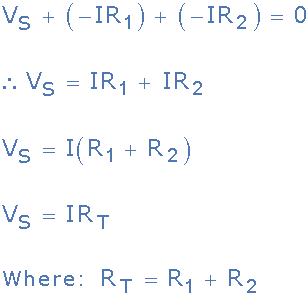
* Kirchhoff’s Voltage Law or KVL, states that “in any closed loop network, the total voltage around the loop is equal to the sum of all the voltage drops within the same loop” which is also equal to zero.
* In other words the algebraic sum of all voltages within the loop must be equal to zero.

**Circuit diagram:**



**Mathematical expression:**

Mathematical expression of kvl for above circuit is,



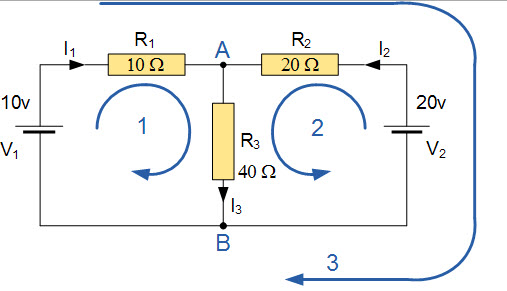
**B) kirchoffs current law:**

* Kirchhoff's Current **Law** (**KCL**) is Kirchhoff's first **law** that deals with the conservation of charge entering and leaving a junction.

**Statement:**

* Kerchief current law states that for a parallel path the total current entering a circuits junction is exactly equal to the total current leaving the same junction.
* In other we can say that The algebraic sum of all currents entering and exiting a node must equal zero.

**Circuit diagram:**



**Mathematical expression:**

Mathematical expressions for above circuit are,

I1+I2+ (-I3) =0

General expression is,

I1+I2+I3…………IN=0

**NOTE:** The current entering the junction will be taken as +ive, while the leaving one will be taken as –ive and vice versa...

C) **OHM’S LAW:**

**Ohm's law** is a **law** that states that the voltage across a resistor is directly proportional to the current flowing through the resistance.

Mathematically:  
 **V= I×R**

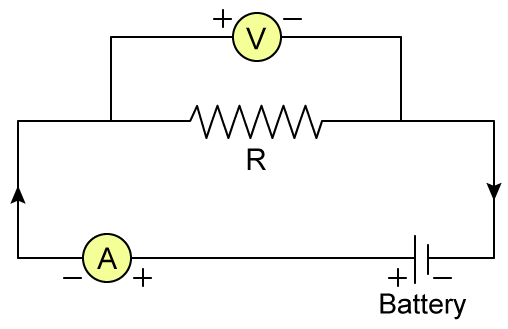
**Where R is constant of propstionality and is called resistance.**

V= voltage, I= current and  R= resistance

The SI unit of resistance is **ohms** and is denoted by **Ω**

**Circuit diagram:**

Ohm's law can be verified using following circuit diagram,

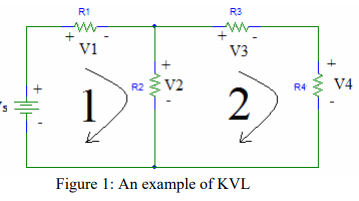


1. **Apparatus used:**

* Breadboard
* Power supply
* Connecting wires
* Resisters
* Multimeter

1. **Procedure:**

* Construct the circuit on bread according to given circuit.



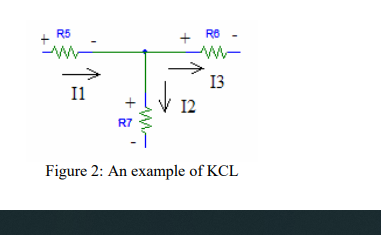
* Connect power supply to the circuit.
* Now change the magnitude of voltage then according to ohm’s law current will also be changed according to given relation by keeping R constant.

V = IR

* Now according to kvl, the sum of all voltages in a closed loop must be zero.If loop 1 is followed clockwise the KVL equation is

V1 +V2 −Vs = 0.

* This equation holds true only if the passive sign convention is satisfied. In the case of KVL the passive sign convention states that when a positive node is encountered while following a loop the voltage across the element is positive. If a negative node is encountered the corresponding element voltage is negative. In order to simplify the KVL equations, the polarities should be assigned to satisfy the passive sign convention whenever possible.
* KCL states that the sum of all currents at a node must equal zero. This is illustrated in given figure.



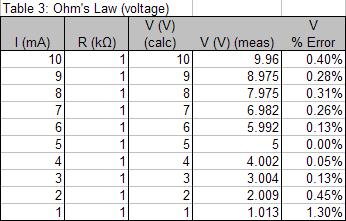
The equation obtained by KCL for the node shown in above Fig. is,

I1 − I 2 − I 3 = 0

* In the case of KCL the passive sign convention deals with the direction of currents with respect to the node. Currents entering the node must have opposite signs as those exiting the node. The passive sign convention with respect to KVL can also be applied to KCL. On many schematics the polarities of resistors are already assigned, so the directions of the currents should be assigned such that the current is entering the positive terminal. This will simplify later calculations.

1. **Observation and calculation:**

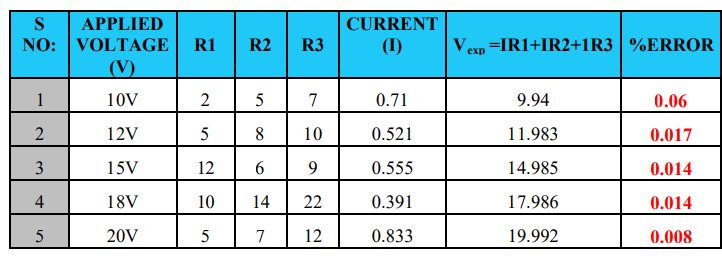
**a)verification of ohm’s law…**

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**b) Verification of KCL law…**

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **S NO** | **VS** | **R1** | **R2** | **R3** | **I1** | **I2** | **I3** | **1I=I2+I3** | measure value | error |
| **1** | 5 | 2.73k | 2k | 1.5k | 1.39mA | 597.3uA | 795.5uA | 795.5+597.3 =1.39mA | 1.28mA | 0.11 |
| **2** | 8 | 1K | 10 | 300 | 10.55A | 7. 55A | 3A | 7.55+3= 10.55 | 10mA | 0.55 |
| **3** | 10 | 700 | 35 | 60 | 6.33mA | 4.22mA | 2.11mA | 4.22m+ 2.11m= 6.33mA | 6.55mA | -0.22 |
| **4** | 15 | 150 | 200 | 300 | 4A | 2.36A | 1.64A | 2.36A+1.64A= 4A | 3.99mA | 0.1 |
| **5** | 20 | 100 | 200 | 1K | 3mA | 2.3mA | 0.7mA | 2.3m+0.7m= 3mA | 3mA | 0.0 |

**c) verification of kvl law:**



1. **Analysis:**

**a)analysis of kcl:**

According Kirchhoff’s Current Law, if the currents entering the junction are taken as positive, while the ones leaving the junction are taken as negative, its algebraic sum will be equal to zero, thus from above data we proved that I1 + I2 +(- I3 )= 0

So we can confirm by analysis that Kirchhoff’s current law (KCL) which states that “the algebraic sum of the currents at a junction point in a circuit network is always zero” is true and correct.

**b) analysis of kvl:**

We have seen here that Kirchhoff’s voltage law, KVL is Kirchhoff’s second law and states that the algebraic sum of all the voltage drops, as you go around a closed circuit from some fixed point and return back to the same point, and taking polarity into account, is always zero.

That is ΣV = 0

**c) analysis of ohm’s law:**

From The Above Experiment We Conclude That Current In A Circuit Is Directly Propositional To Voltage By Keeping Resistance Constant. THIS is also verified from above graph. From ohm’s law it is cleared that in case of metallic conductor there will be direct relation b/w current and voltage by keeping other physical condition constant.

**THE END**